Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. **(currently amended)** A method of manufacturing semiconductor devices, comprising the steps of:

forming a plurality of gates on a semiconductor substrate;

forming one or more p+ source/drain junctions in the semiconductor substrate by implanting first ions;

forming an insulation layer on an entire surface of the semiconductor substrate to coat the plurality of gates;

selectively removing the insulation layer by using a first mask pattern to form a **plurality of** contact hole**s**, which expose~~s a~~ **at least one** source/drain junction and a conductive layer ~~**in a portion**~~ **of at least one** of the **plurality of** gates in the semiconductor substrate;

removing the first mask pattern and forming a second mask pattern on the selectively removed insulation layer, the second mask pattern exposing **only one or more** the p+ source/drain junction**s** in the semiconductor substrate;

implanting **dopant** ion**s again** into **one or more of** the p+ source/drain junction**s** in the semiconductor substrate by using the second mask pattern as a mask;

removing the second mask pattern and rapid thermal annealing the entire

substrate in an activation temperature range of dopant which is implanted in the ion implantation step; and

burying the contact holes with conductive material to form a bit line contact plug **in each contact hole**.

2. (original) The method of manufacturing semiconductor devices according to claim 1, wherein the ion implantation step is performed with the dose of $4.5\sim6\times10^{15}$ atoms/cm^2.

3. (original) The method of manufacturing semiconductor devices according to claim 1, wherein the ion implantation step is performed with the energy of 10~24keV.

4. (original) The method of manufacturing semiconductor devices according to claim 1, wherein a tilt angle is adjusted in a range of about 0 to 60 degrees in the ion implantation step.

5. (original) The method of manufacturing semiconductor devices according to claim 1, wherein an orientation is adjusted in a range of about 0 to 90 degrees in the ion implantation step.

6. (**currently amended**) The method of manufacturing semiconductor devices according to claim 1, wherein rotation is adjusted ~~within~~ **zero to** four times ~~in~~ **during** the ion implantation step.

7. (original) The method of manufacturing semiconductor devices according to claim 1, wherein the rapid thermal annealing is performed at a temperature of 830°C or less.

8. (**currently amended**) The method of manufacturing semiconductor devices according to claim 7, wherein the rapid thermal annealing uses 1 to 25slm N_2 gas as a purge gas.

9. (original) The method of manufacturing semiconductor devices according to claim 7, wherein the rapid thermal annealing is performed at a heating rate of about 10 to 100°C/sec.